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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,386	11/14/2003	Andrew H. Barr	200308581-1	3950

22879 7590 08/06/2008

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ART UNIT	PAPER NUMBER
2863	

NOTIFICATION DATE	DELIVERY MODE
08/06/2008	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/714,386
Filing Date: November 14, 2003
Appellant(s): BARR ET AL.

Christopher P. Kosh
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/20/2008 appealing from the Office action mailed 1/11/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2003/0115385 Adamane 6-2003

Merriam Webster's online dictionary, Definition of "operating system"

http://www.merriam-webster.com/dictionary/operating%20system

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamane et al. (USPN 2003/0115385).

With regards to claim 1, Adamane et al. (USPN 2003/0115385) teaches a computer system comprising: a processor(101) configured to execute an operating system;(Page 2, paragraph 0022)

a memory controller coupled to the processor;(101;fig 1)

a memory coupled to the memory controller;(101,104,108;fig 1)

a first input/output (I/O) controller coupled to the memory controller;(101,118 fig1)

a first expansion slot coupled to the first I/O controller;(101,118;fig 1) and

a test module directly coupled to the first expansion slot; (Page 1, paragraph 0005)

wherein the test module is configured to obtain access to a portion of the memory from the operating system, and wherein the test module is configured to cause tests to be

performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 2, Adamane et al. (USPN 2003/0115385) teaches the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory subsequent to the operating system being booted. (Page 1, paragraph 0011 &0015)

With regards to claim 3, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause the tests to be performed on the portion of the memory during execution of the operating system. (Page 1, paragraph 0011 &0015)

With regards to claim 4, Adamane et al. (USPN 2003/0115385) teaches a second I/O controller coupled to the memory controller; a second expansion slot coupled to the second I/O controller; and an I/O device coupled to the second expansion slot.(fig 1)

With regards to claim 5, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/O controller. (Page 2, paragraph 0023)

With regards to claim 6, Adamane et al. (USPN 2003/0115385) teaches the read and write transactions
comprise DMA transactions. (Page 1, paragraph 0023)

With regards to claim 7, Adamane et al. (USPN 2003/0115385) teaches a bus bridge coupled to the processor and the first I/O controller. (114; fig 1)

With regards to claim 8, Adamane et al. (USPN 2003/0115385) teaches a system controller that comprises the memory controller. (101; fig 1)

With regards to claim 9, Adamane et al. (USPN 2003/0115385) teaches obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system; (Page 1, paragraph 0015)
generating a test transaction in a test module directly coupled to an expansion slot of the computer system; (Page 1, paragraph 0004 & 0015) and
providing the test transaction to the portion using direct memory access (DMA) to cause information to be read from or stored into the portion subsequent to obtaining access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 10, Adamane et al. (USPN 2003/0115385) teaches detecting an error that occurs in response to the test transaction; and performing a remedial action associated with the portion in response to detecting the error. (Page 1, paragraph 0015)

With regards to claim 11, Adamane et al. (USPN 2003/0115385) teaches providing the test transaction from the test module to an I/O controller coupled to the expansion slot; (118 fig 1)
providing the test transaction from the I/O controller to a bus bridge;(114 fig 1)
providing the test transaction from the bus bridge to a system bus; (112 fig 1)
providing the test transaction from the system bus to a memory controller; (101 fig 1)and
providing the test transaction from the memory controller to the portion. (104,106; fig 1)

With regards to claim 12, Adamane et al. (USPN 2003/0115385) teaches storing information in the memory in response to the test transaction being a write transaction. (Page 2, paragraph 0021)

With regards to claim 13, Adamane et al. (USPN 2003/0115385) teaches in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller; (Page 1, paragraph 0015) providing the information from the memory controller to the system bus; providing the information from the system bus to the bus bridge; providing the information from the bus bridge to the I/O controller; and providing the information from the I/O controller to the test module. (see fig 1)

With regards to claim 14, Adamane et al. (USPN 2003/0115385) teaches providing the test transaction from the test module to an I/O controller coupled to the expansion slot; providing the test transaction from the I/O controller to a system controller; providing the test transaction from the system controller to a memory controller; and providing the test transaction from the memory controller to the portion. (fig 1)

With regards to claim 15, Adamane et al. (USPN 2003/0115385) teaches computer system comprising:

a processor ;(101 fig 1)

a memory controller coupled to the processor and configured to perform error correction ;(101 fig 1)

a memory coupled to the memory controller ;(fig 1)

an input/output (I/O) controller coupled to the memory controller ;(101,118; fig 1)

an expansion slot coupled to the I/O controller; 118 and

a card directly coupled to the expansion slot; (Page 1, paragraph 0004)

wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 16, Adamane et al. (USPN 2003/0115385) teaches the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted. (Page 1, paragraph 0011 & 0015)

With regards to claim 17, Adamane et al. (USPN 2003/0115385) teaches the operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system. (Page 1, paragraph 0011 &0015)

With regards to claim 18, Adamane et al. (USPN 2003/0115385) teaches the I/O controller provides the read transactions to a system bus. (fig 1)

With regards to claim 19, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA). (Page 1, paragraph 0015)

With regards to claim 20, Adamane et al. (USPN 2003/0115385) teaches the read transactions comprise direct memory access (DMA) transactions. (Page 1, paragraph 0015)

Adamane et al does not appear to explicitly teach a test module card.

Adamane et al does teach I/O cards (Page 1, paragraph 0004) and testing a I/O device. (Page 1, paragraph 005)

It would've been obvious to one skilled in the art at the time of the invention to use a test module card to test the I/O device in order to determine that it is functioning normally.

(10) Response to Argument

APPELLANT'S ARGUMENTS:

A. Rejection of Claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Adamane

(I *Appellant's argument*) Applicable law section.

In this section appellant cites the criteria set forth by 35 U.S.C 103 to establish a prima facie case of obviousness.

(I - *Examiner's response*)

Examiner has met the burden to establish a prima facie case of obviousness. The claimed invention is clearly obvious in view of the Adamane et al. (USPN 2003/0115385) reference.

(II- *Appellant's argument*)

Rejections of claims 1-20 under 35 U.S.C 103 (a) as being unpatentable over U.S Patent publication 2003/0115385 (Adamane et al.). Adamane et al. does not teach or suggest all the limitation of claims 1-20

(II - *Examiner's response*)

Adamane et al. clearly teaches and suggests all the limitation of claims 1-20. Please refer to the Rejections of claims 1-20 under 35 U.S.C 103 (a) cited above.

(II a- *Appellant's argument*)

Adamane does not teach or suggest "a test module card directly coupled to the first expansion slot", "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" or "wherein the test module card is

configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 1.

(II a- *Examiner's response*)

Paragraph 15 of the Adamane et al. reference clearly teaches input/output (I/O) devices (test card is an I/O device) that are configured to obtain access to a portion of the memory from the operating system. Further it should be noted that the computer architecture in both the prior art and appellant's invention require some sort of operating system in order to test the memory. A operating system is merely a set of instructions that enable the computer hardware to perform desired functions. Therefore, it would be inherent for the both system to have an operating system as they are both performing a function. Please see paragraph 0015 of the Adamane et al. reference below.

> **[0015]** In a preferred embodiment of the present invention, I/O devices **118** are testing devices that stress test computer system **100** by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory **104** (and by implication main memory **106**). I/O devices **118** perform repeated DMA transfers while varying transfer parameters pseudo-randomly so as to simulate the behavior of many different types of I/O devices. Also, processors **101** may also access cache memory **104** concurrently, so as to place further stress on computer system **100**. The resulting contents of cache memory **104** and/or main memory **106** can then be examined to observe the effects of varying DMA parameters and concurrent memory access between I/O devices **118** and processors **101**. DMA transfer parameters that may be varied include start address alignment, transfer size, transfer width, byte lane enables, request assertion time, request deassertion time, number of wait states, number of idle states, disconnect count, retry limit, bus commands, and whether to override a latency timer. In addition, I/O devices **118** may issue any other possible bus commands.

Appellant goes on to argue that the Adamane reference does not teach the test module device is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory Please see paragraph 0015 of the Adamane et al. reference.

Paragraph 0015 does not explicitly state that the I/O testing devices are test module cards. Paragraph 004 of the Adamane et al. reference (see below) does teach I/O functions are performed through the use of cards. Therefore the examiner has taken the position that the use of I/O card to test the memory would be an obvious modification and would meet the requirements set forth by 35 U.S.C 103.

[0004] Modern computer systems rely on a large number of input/output (I/O) devices, for exchanging data with human users, for storing data, and for communicating with other computer systems, among other tasks. In many computer systems, I/O is performed through the use of I/O cards that plug into slots connected to a backplane bus, such as a peripheral component interconnect (PCI) bus. These different I/O cards have varying features and capabilities. For this reason, many permutations and combinations of I/O cards may be possible within a single computer system. With the potential use of such a large number of I/O cards, it is a significant challenge to test a computer I/O subsystem. Furthermore, it is not always possible to foresee and predict all of the I/O cards that need to be used on a given bus system. This is especially apparent if the bus associated with the I/O subsystem is an open industry standard bus system like PCI. Thus there is a need to be able to easily test computer I/O sybsystem by subjecting such subsystems to a variety of different "irritations" representative of a large number of combinations and permutations of possible I/O devives within the system.

(II b- *Appellant's argument*)

Appellant argues that the Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card.

(II b- *Examiner's response*)

Paragraph 0015, detailed description of the Adamane et al. reference does not explicitly teach that the I/O testing devices are test module cards. Paragraph 004 of the Adamane et al. reference does teach I/O functions are performed through the use of cards. Therefore the examiner has taken the position that the use of I/O card to test the memory would be an obvious modification and would meet the requirements set forth by 35 U.S.C 103.

(II c- *Appellant's argument*)

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1.

(II c - *Examiner's response*)

Paragraph 0015 of the Adamane reference clearly teaches I/O testing devices. Paragraph 004 of the Adamane et al clearly teaches that I/O is performed through the use of I/O cards.

In appellants invention the first expansion slot is an I/O slot where the test module card is to be directly coupled to the computer system through the slot.

Obviously the I/O card taught by Adamane would be directly coupled to the I/O slot. For example a CD would not be coupled to the disk drive of a computer it would obviously be coupled to the CD-ROM drive.

It is the examiners position that the Adamane et al. reference teaches a test module card directly coupled to the first expansion slot.

(II d- *Appellant's argument*)

In addition, Adamane does not teach or suggest "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 1. The Examiner also cites paragraph [0015] of Adamane as a teaching of this feature of claim 1. Final Office Action, p. 2. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

(II d- *Examiner's response*)

Note paragraph 0011 of Adamane et al.

> [0011] **FIG. 1** is a block diagram depicting a computer system **100** in which a preferred embodiment of the present invention may be implemented. A number of processors **101** reside on a local bus **102**, as well as a cache memory **104**, which serves as a high-speed temporary storage location for data located in main memory **106**. Processors **100** process functional descriptive material that is encoded into a computer-readable medium such as main memory **106**. Functional descriptive material may include, but is not limited to, computer programs and information structures. Functional descriptive material may comprise a set of instructions, or they may comprise constraints, rules, or other constructs imparting functionality to computer system **100** when processed by processors **101**.

clearly illustrates that the processors use functional descriptive material i.e. computer programs and information structures in order to impart functionality to a computer system. As previously discussed a operating system is merely a set of instructions that impart functionality. Paragraph 0015 of Adamane et al. (see above) teaches that the I/O testing devices perform tests on the memory using direct memory access (DMA). Clearly, a portion if not all the memory is accessed as it is being tested.

Furthermore, the operating system/functional descriptive material must be stored in a memory and the memory is what is being tested. Please refer to Paragraph 0011 recites "processors 100 process functional descriptive material that is encoded into a computer readable medium such as main memory 106"

It is the examiners position that the Adamane et al. reference teaches the test module card is configured to obtain access to a portion of the memory from the operating system

(II e- *Appellant's argument*)

Appellant argues that the Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Webster's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of" wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 1.

(II e- *Examiner's response*)

In the final office action, "Merriam Webster's online dictionary" was used in examiners response to appellant's arguments in order to clarify examiners position on the definition of a "operating system". In no way is Merriam Webster definition relied upon for the 35 USC 103 rejection in view of Adamane et al. The definition was introduced into examiners arguments as it was unclear whether appellant understood examiners interpretation of the meaning of an "operating system".

The Merriam Webster's definition has been cited on a Notice of References Cited (PTO-892) and has been sent to appellant in a supplemental communication (mailed 07/15/2008).

As appellant has introduced this reference into the appeal brief, examiner has cited the definition in *section (8) evidence relied upon* of the examiners answer.

Further paragraphs 0011 & 0015 in combination of Adamane clearly teach wherein the test module card is configured to obtain access to a portion of the memory from the operating system.

It is the examiners position that the Adamane et al. reference solely discloses all the claimed elements of appellant's invention.

(II f- *Appellant's argument*)

Further, Appellant argues that Adamane does not teach or suggest "wherein the test module card is configured *to cause tests to be performed on the portion of the memory* using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 1 (emphasis added). The Examiner cites paragraph [0015] of Adamane as a teaching of this feature of claim 1. Final Office Action, p. 2. Paragraph [0015] of Adamane, however, does not support that notion that tests are "performed on the portion of the memory" as recited in claim 1. Instead, Adamane teaches away from this feature of claim 1 by teaching that "the present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system." Adamane, paragraph [0005], lines 1-3.

(II f- *Examiner's response*)

Appellant argues that the Adamane reference does not teach the test module device is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. Please see paragraph 0015 of the Adamane et al. reference.

The Adamane reference teaches memory testing. This is sufficient to meet the claim limitation as Adamane teaches testing at least a portion of the memory.

Appellant cites paragraph 005 of Adamane and alleges that the this section teaches away from appellants invention. Examiner respectfully disagrees that this section teaches away from appellant's invention. Clearly the stress testing taught by the Adamane et al. reference teaches testing I/O subsystem of the computer system and in doing so the memory is also tested using DMA.

SUMMARY OF THE INVENTION

[0005] The present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system. An input/output device capable of engaging in repetitive direct memory access (DMA) transfers with pseudo-randomized transfer parameters is allowed to execute multiple DMA transfers with varying parameters. In this way, a single type of device may be used to simulate the effects of multiple types of devices. Multiple copies of the same I/O device may be used concurrently in a single computer system along with processor software to access the same portions of memory. In this way, false sharing, true sharing may be effected.

It is the examiners position that the Adamane et al. reference teaches the test module device is configured to cause tests to be performed on the portion of the

memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

B. Rejections of claims 9-14 under 35 U.S.C 103 (a) as being unpatentable over Adamane et al.

(I- *Appellant's argument*)

Appellant argues that Adamane does not teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9. The Examiner cites paragraph [0015] of Adamane as a teaching of this feature of claim 9. Final Office Action, p. 4. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

(I- *Examiner's response*)

As described in paragraph 0011(see above) of the Adamane et al. reference functional descriptive material is defined as a set of instructions or they may comprise constraints, rules or other constructs imparting functionality to a computer system 100 when processed by processors 101. This description of a operating system is functionally equivalent to an operating system. As described above in paragraph 0015 of Adamane "I/O devices 118 are testing devices that stress test computer system 100 by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory 104... Clearly the computer system of Adamane has an operating system, which must interact with the I/O device in order to test the memory. Further the computer system taught by Adamane must be in operation as a "stress" test

is performed on the computer system. As the computer is "stressed" there must be some sort of operation in the computer system in order for the test to be conducted.

Further paragraphs 0021-0022 (see below) of Adamane et al. describe the stress testing in more detail.

[0021] **FIG. 2** is a block diagram of an I/O device **200** for stress testing a computer system in accordance with a preferred embodiment of the present invention. I/O device **200** could be, for instance, one of I/O devices **118** in **FIG. 1**. Embedded processor **202** resides on local device bus **204**, through which is accesses memory **206**. Memory **206** stores functional descriptive material that defines the operation of I/O device **200**. Memory **206** is preferably some kind of non-volatile memory for storing functional descriptive material as firmware. The functional descriptive material contained in memory **206** enables embedded processor **202** to engage in DMA writes and reads to computer system memory through PCI bus interface **208**. Embedded processor **202** randomizes DMA transfer parameters and conducts repetitive DMA transfers. The operation of I/O device **200** according to the functional descriptive material in memory **206** is further described in **FIGS. 3 and 4**.

[0022] **FIG. 3** is a functional block diagram depicting a process of randomization of DMA transfer parameters **300** in an I/O device in accordance with a preferred embodiment of the present invention. The steps depicted in **FIG. 3** are preferably performed as steps in a software program incorporated into functional descriptive material stored in memory **206** or I/O device **200**. Which parameters are to be randomized (**302**) is provided as input to the I/O device from software operating on at least one of processors **101** (**FIG. 1**). Parameter selection code **304** selects values for the varied parameters based on random numbers provided by random number generator **306**, which may be implemented in hardware or software. The randomized DMA transfer parameters (**308**) are then provided as input to DMA access code **310**, which effects a DMA transfer (i.e., a write or read) according to the provided parameters. The results of false/true sharing done between processors **101** and the DMA from I/O device **200**, are verified by software operating on processors **101**.

(I a- *Appellant's argument*)

Appellant argues that the Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Webster's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9.

(I a- *Examiner's response*)

In the final office action, "Merriam Webster's online dictionary" was used in examiners response to appellant's arguments in order to clarify examiners position on the definition of a "operating system". In no way is Merriam Webster definition relied upon for the 35 USC 103 rejection in view of Adamane et al. The definition was introduced into examiners arguments as it was unclear whether appellant understood examiners interpretation of the meaning of an "operating system".

The Merriam Webster's definition has been cited on a Notice of References Cited (PTO-892) and has been sent to appellant in a supplemental communication.

As appellant has introduced this reference into the appeal brief, examiner has cited the definition in *section (8) evidence relied upon* of the examiners answer.

Further paragraphs 0011 & 0015 in combination of Adamane clearly teach obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system.

It is the examiners position that the Adamane et al. reference solely discloses all the claimed elements of appellant's invention.

(I b -*Appellant's argument*)

Appellant argues that the Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card." Final Office Action mailed January 11, 2008, p. 7 (hereafter Final Office Action).

(I b- *Examiner's response*)

Paragraph 0015 does not explicitly teach that the I/O testing devices are test module *cards*. Paragraph 004(background of invention) of the Adamane et al. reference does teach I/O functions are performed through the use of cards. Therefore the examiner has taken the position that the use of I/O card to test the memory would be an obvious modification and would meet the requirements set forth by 35 U.S.C 103.

(I c- *Appellant's argument*)

Appellant argues that the Examiner, however, attempts to overcome this deficiency by citing "I/O cards" in the BACKGROUND OF THE INVENTION section of Adamane (paragraph [0004]) and "testing a (sic) I/O device" in paragraph [0015] of Adamane. Final Office Action, pp. 7-8.

(I c- *Examiner's response*)

Clearly, the Adamane reference teaches I/O devices are testing device and paragraph 0004 of Adamane teaches in many computer systems, I/O is performed through the use of I/O cards that plug into slots… Examiner conceding that the paragraph 0015 does not explicitly teach that the I/O testing devices are cards.

However, it is obvious to one skilled in the art at the time of the invention to use a I/O test card in order to test the computer system of Adamane et al. Paragraph 004 background of invention of the Adamane reference was used in order provide evidence that using a I/O card is obvious to one of ordinary skill in that art.

(I d- *Appellant's argument*)

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "generating a test transaction in a test module card directly coupled to an expansion slot of the computer system" as recited in claim 9.

(I d- *Examiner's response*)

Paragraph 0015 of the Adamane reference clearly teaches I/O *testing* devices. Paragraph 004 of the Adamane et al clearly teaches that I/O is performed through the use of I/O cards.

In appellants invention the first expansion slot is an I/O slot where the test module card is to be directly coupled to the computer system through the slot.

Obviously the I/O card taught by Adamane would be directly coupled to the I/O slot. For example a CD would not be coupled to the disk drive of a computer it would obviously be coupled to the CD-ROM drive.

It is the examiners position that the Adamane et al. reference teaches a test module card directly coupled to the first expansion slot.

(I e- *Appellant's argument*)

Adamane does not teach or suggest the above features of claim 9. Accordingly, Appellants respectfully request the reversal of the rejection of claim 9 and claims 10-14 which depend from claim 9 under 35 U.S.C. § 103(a) for at least this reason.

(I e- *Examiner's response*)

It is the examiners position that the Adamane et al. reference teaches each and every element of appellant's invention.

C. Rejections of claims 15-20 under 35 U.S.C 103 (a) as being unpatentable over Adamane et al.

(I - *Appellant's argument*)

Adamane does not teach or suggest "a test module card directly coupled to the expansion slot", "wherein the test module card is configured to obtain access to a portion of the memory from an operating system", or "wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory" as recited in claim 15.

(I- *Examiner's response*)

Paragraph 15 of the Adamane et al. reference teaches clearly teaches I/O devices that are configured to obtain access to a portion of the memory from the operating system. Further it should be noted that the computer architecture in both the prior art and appellant's invention require some sort of operating system in order to test the memory. A operating system is merely a set of instructions that enable the computer

hardware to perform desired functions. Therefore, it would be inherent for the both system to have an operating system as they are both performing a function. Please see paragraph 0015 of the Adamane et al. reference.

Appellant goes on to argue that the Adamane reference does not teach the test module device is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory Please see paragraph 0015 of the Adamane et al. reference below.

Paragraph 0015 does not explicitly teach that the I/O testing devices are test module cards. Paragraph 004 of the Adamane et al. reference does teach I/O functions are performed through the use of cards. Therefore the examiner has taken the position that the use of I/O card to test the memory would be an obvious modification and would meet the requirements set forth by 35 U.S.C 103.

(I a- *Appellant's argument*)

Appellant argues that the Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card." Final Office Action mailed January 11, 2008, p. 7 (hereafter Final Office Action).

(I a- *Examiner's response*)

Paragraph 0015 does not explicitly teach that the I/O testing devices are test module *cards*. Paragraph 004(background of invention) of the Adamane et al. reference does teach I/O functions are performed through the use of cards. Therefore the

examiner has taken the position that the use of I/O card to test the memory would be an obvious modification and would meet the requirements set forth by 35 U.S.C 103.

(I b- *Appellant's argument*)

Appellant argues that the Examiner, however, attempts to overcome this deficiency by citing "I/O cards" in the BACKGROUND OF THE INVENTION section of Adamane (paragraph [0004]) and "testing a (sic) I/O device" in paragraph [0015] of Adamane. Final Office Action, pp. 7-8.

(I b- ***Examiner's response***)

Clearly, the Adamane reference teaches I/O devices are testing device and paragraph 0004 of Adamane teaches in many computer systems, I/O is performed through the use of I/O cards that plug into slots... Examiner conceding that the paragraph 0015 does not explicitly teach that the I/O testing devices are cards. However, it is obvious to one skilled in the art at the time of the invention to use a I/O test card in order to test the computer system of Adamane et al. Paragraph 004 background of invention of the Adamane reference was used in order provide evidence that using a I/O card is obvious to one of ordinary skill in that art.

(I c- *Appellant's argument*)

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 15.

(I c- *Examiner's response*)

Paragraph 0015 of the Adamane reference clearly teaches I/O *testing* devices. Paragraph 004 of the Adamane et al clearly teaches that I/O is performed through the use of I/O cards.

In appellants invention the first expansion slot is an I/O slot where the test module card is to be directly coupled to the computer system through the slot.

Obviously the I/O card taught by Adamane would be directly coupled to the I/O slot. For example a CD would not be coupled to the disk drive of a computer it would obviously be coupled to the CD-ROM drive.

It is the examiners position that the Adamane et al. reference teaches a test module card directly coupled to the first expansion slot.

(I d- *Appellant's argument*)

In addition, Adamane does not teach or suggest "wherein the test module card is configured to obtain access to a portion of the memory from an operating system" as recited in claim 15. The Examiner cites paragraph [0015] of Adamane as a teaching of this feature of claim 15. Final Office Action, p. 6. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

(I d- *Examiner's response*)

As described in paragraph 0011(see above) of the Adamane et al. reference functional descriptive material is defined as a set of instructions or they may comprise constraints, rules or other constructs imparting functionality to a computer system 100

when processed by processors 101. This description of a operating system is functionally equivalent to an operating system. As described above in paragraph 0015 of Adamane "I/O devices 118 are testing devices that stress test computer system 100 by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory 104... Clearly the computer system of Adamane has a operating system, which must interact with the I/O device in order to test the memory. Further the computer system taught by Adamane must be in operation as a "stress" test is performed on the computer system. As the computer is "stressed" there must be some sort of operation in the computer system in order for the test to be conducted.

Further paragraphs 0021-0022 of Adamane et al. describe the stress testing in more detail.

(I e- *Appellant's argument*)

Appellant argues that the Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Webster's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of" wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 15.

(I e- *Examiner's response*)

In the final office action, "Merriam Webster's online dictionary" was used in examiners response to appellant's arguments in order to clarify examiners position on

the definition of a "operating system". In no way is Merriam Webster definition relied upon for the 35 USC 103 rejection in view of Adamane et al. The definition was introduced into examiners arguments as it was unclear whether appellant understood examiners interpretation of the meaning of an "operating system".

The Merriam Webster's definition has been cited on a Notice of References Cited (PTO-892) and has been sent to appellant in a supplemental communication (as explained above).

As appellant has introduced this reference into the appeal brief, examiner has cited the definition in *section (8) evidence relied upon* of the examiners answer.

Further paragraphs 0011 & 0015 in combination of Adamane clearly teach obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system.

It is the examiners position that the Adamane et al. reference solely discloses all the claimed elements of appellant's invention.

(I f- *Appellant's argument*)

Further, Adamane further does not teach or suggest "wherein the test module card is configured *to cause tests" to be performed on the portion of the memory* by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory" as recited in claim 15 (emphasis added). The Examiner again cites paragraph [0015] of Adamane as a teaching of this feature of claim 15. Final Office Action, p. 6. Paragraph [0015] of Adamane, however, does not support that notion that tests are "performed on the portion of the memory" as

recited in claim 15. Instead, Adamane teaches away from this feature of claim 15 by teaching that "It]he present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system." Adamane, paragraph [0005], lines 1-3.

(I f- *Examiner's response*)

Appellant argues that the Adamane reference does not teach the test module device is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. Please see paragraph 0015 of the Adamane et al. reference.

The Adamane reference teaches memory testing. This is sufficient to meet the claim limitation as Adamane teaches testing at least a portion of the memory.

It is the examiners position that the Adamane et al. reference teaches the test module device is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

Appellant cites paragraph 005 of Adamane and alleges that the this section teaches away from appellants invention. Examiner respectfully disagrees that this section teaches away from appellant's invention. Clearly the stress testing taught by the Adamane et al. reference teaches testing I/O subsystem of the computer system and in doing so the memory is also tested using DMA.

(I g- *Appellant's argument*)

Adamane does not teach or suggest the above features of claim 15. Accordingly, Appellants respectfully request the reversal of the rejection of claim 15 and claims 16-20 which depend from claim 15 under 35 U.S.C. § 103(a) for at least this reason.

(I g- *Examiner's response*)

It is the examiners position that the Adamane et al. reference teaches each and every element of appellant's invention.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Aditya Bhat/

Examiner, Art Unit 2863

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